D. Drawings

Please enter the four attached replacement sheets, which effectively delete reference numeral 240 from Fig. 1, reference numerals 201 and 202 from Figs. 2A, 2B and 3, and reference numerals 5003, 5010 and 5014 from Fig. 5.

E. Remarks

The claims are 1-8, with claim 1 being the sole independent claims. Claims 2-7 have been amended to make certain formal corrections. Each amendment made to the claims is supported by the application as filed; accordingly, no new matter has been added. Reconsideration of this application is respectfully requested.

The Examiner objected to the drawings as failing to comply with 37 C.F.R. 1.84(p)(5) because they do not include reference numerals 706a and 5000 which are mentioned in the specification. In addition, the Examiner objected to the drawings on the same basis because they do include reference numerals 240, 201, 202, 5003, 5010 and 5014, which are not mentioned in the specification. In response, Applicants have deleted each of reference numerals 706a and 5000 from the specification and each of reference numerals 240, 201, 202, 5003, 5010 and 5014 from the figures. Accordingly, Applicants respectfully request removal of the objections to the drawings.

The Examiner objected to claim 4 due to its use of the term "input unit". In response, Applicants have amended claim 4 to replace "input unit" with --input line--. The terminology is now consistent throughout the claims. Accordingly, Applicants respectfully request removal of the objection to claim 4.

Claims 1, 2 and 6-8 stand rejected under 35 U.S.C. §102(b) as being anticipated by Imanaka (U.S. Patent No. 6,243,111). Claims 3-5 stand rejected under 35 U.S.C. §103(a) as being obvious over Imanaka in view of Ghozeil (U.S. Patent No. 6,375,295). Applicants respectfully traverse these rejections.

At the outset, Applicants would like to direct the Examiner's attention to the present specification at pages 4-6 where the following distinguishing treatment of Imanaka is set forth:

Thus, USP 6,243,111 discloses a configuration for shifting a drive pulse, which is applied to heating elements belonging to an identical block, little by little for each heating element. That is, in forming an ink jet head substrate, a hysteresis circuit is provided in an input section together with components for a logic discharge control circuit such as heating elements, a driver, and a shift register and, at the same time, a CR (capacitor resistor) integrating circuit is formed in a signal path for a heat pulse (input pulse width signal), which regulates a pulse width and timing of a drive pulse, such that the drive pulse is applied to different heating elements at staggered timing. Consequently, the heat pulse is delayed to drive the respective heating elements sequentially. In this way, timing of the heat pulse is staggered using the CR integrating circuit, and a current flowing to the heating elements is controlled, whereby the number of heating elements which are turned ON at exactly the same timing is reduced, and a peak value of a current or a rising ratio of a current due to the drive pulse is reduced to suppress generation of noises. Consequently, even if there is increase in the number of heating elements which are driven simultaneously due to increase in the number of discharge ports or high-density implementation of discharge ports indispensable for high-speed printing, generation of inductive noises or the like can be suppressed.

However, in the case in which generation of noises is suppressed by using the CR integrating circuit as disclosed in USP 6,243,111, if there are fluctuations in C (capacitance) and R (resistance), a product of the fluctuations results in a fluctuation in a delay value of the heat pulse. Thus, a current flowing to the heating elements cannot be controlled with high accuracy and, as a result, generation of noises cannot be suppressed sufficiently. In addition, since the CR integrating circuit is constituted by an input buffer, a capacitor, and a resistor, when a difference of a wiring pattern length to a logic circuit input of the next stage increases, the delay value fluctuates. In addition, in the head substrate which is typically manufactured using a silicon semiconductor device manufacturing technique, a gate oxide film is often used for a capacitor and a diffused resistor is often used as a resistor. When it is intended to constitute a CR integrating circuit having a desired time constant, the capacitor and the resistor occupy a large area on the head substrate, and the head substrate is enlarged.

The above discussion of Imanaka clearly sets forth the differences between its disclosure and the presently claimed invention. Most importantly, the delay circuit disclosed in Imanaka is a CR integration circuit. Such a circuit comprises a resistor formed by a diffusion region in a semiconductor substrate and a capacitor formed by a gate insulating film of a transistor. Such a circuit is different from the logic circuit employed in the present invention and set forth in sole independent claim 1 of the present application. The logic circuit according to the present invention is a "circuit which determines the output signal, according to an input signal" (page 9, lines 14-16). It may consist of a diode and a transistor (so-called "DTL" (Diode-Transistor Logic)), or it may consist of a transistor instead of the diode (so-called "TTL" (Transistor-Transistor Logic)). In any event, the logic circuit of the present invention is clearly different from the CR integration circuit according to Imanaka. Furthermore, as outlined in the latter part of the specification's discussion of Imanaka, use of a CR integration circuit leads to many performance-related problems due to variation of the delay value. On the other hand, according to the present invention, the use of a logic circuit suppresses the undesirable variation of delay value. Accordingly, Imanaka cannot anticipate the present invention, as it fails to disclose the logic circuit employed therein.

Ghozeil does not remedy the deficiencies of Imanaka. In fact, Ghozeil is cited for its disclosure related to CMOS inverters of even number stages arranged serially. Ghozeil, not unlike Imanaka, does not disclose or suggest the logic circuit of the present invention in its most basic sense. Accordingly, no combination of Imanaka and Ghozeil renders the present invention obvious.

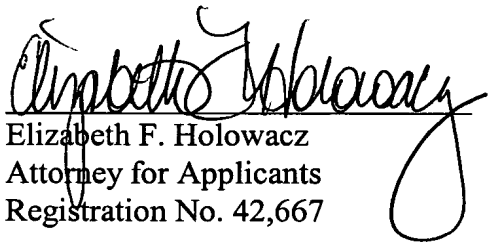
It is clear that neither of the cited references, whether considered alone or in combination, discloses or renders obvious the present invention. There is simply no

teaching of a key feature of the present invention, namely the logic circuit as required in claim 1 of the present application. Accordingly, Applicants respectfully request withdrawal of the prior art rejections.

In view of the foregoing amendments and remarks, favorable reconsideration and passage to issue of the present case is respectfully requested. Should the Examiner believe that issues remain outstanding, the Examiner is respectfully requested to contact Applicants' undersigned attorney in an effort to resolve such issues and advance the case to issue.

Applicants' undersigned attorney may be reached in our New York office by telephone at (212) 218-2100. All correspondence should continue to be directed to our below listed address.

Respectfully submitted,



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